IN THE CLAIMS:

1. (Currently Amended) A method of forming a field effect transistor, the method comprising:

forming an implantation mask over a crystalline semiconductor region;

forming a drain region and a source region ~~using~~ adjacent said implantation mask, said drain and source regions each having a top surface located above a top surface of said crystalline semiconductor region;

removing said implantation mask to expose a surface area of said top surface of said crystalline semiconductor region;

forming a gate insulation layer on said exposed surface area of said top surface of said crystalline semiconductor region;

forming a gate electrode on said gate insulation layer; and

doping said gate electrode.

2. (Original) The method of claim 1, wherein forming said gate electrode includes depositing a gate electrode material above said gate insulation layer and removing excess material of said gate electrode material to form the gate electrode.

3. (Original) The method of claim 1, wherein a lateral size of said implantation mask is greater than a design value of a gate length of said gate electrode.

4. (Currently Amended) The method of claim 1, wherein forming said drain and source regions <u>adjacent said implantation mask</u> includes epitaxially growing a crystalline semiconductor layer adjacent to said implantation mask.

5. (Original) The method of claim 4, wherein a first implantation sequence for forming said drain and source regions is performed prior to epitaxially growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially growing the semiconductor layer.

6. (Original) The method of claim 5, further comprising performing an anneal process to activate said dopants.

7. (Original) The method of claim 6, wherein said anneal process is controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region.

8. (Original) The method of claim 7, wherein said anneal process includes a first anneal cycle performed after said first implantation sequence and prior to said second implantation sequence, said first anneal cycle being configured to substantially completely re-crystallize amorphized portions in said semiconductor region.

9. (Original) The method of claim 3, further comprising forming sidewall spacers on sidewalls of said drain and source regions that are exposed by removing said implantation mask.

10. (Original) The method of claim 9, wherein a width of said sidewall spacers is controlled on the basis of a target gate length for said gate electrode.

11. (Original) The method of claim 1, wherein said implantation mask is removed by an isotropic etch process.

12. (Original) The method of claim 2, wherein said excess material is removed by chemical mechanical polishing.

13. (Original) The method of claim 2, wherein said excess material is removed by an etch process.

14. (Original) The method of claim 2, wherein said excess material is removed by chemical mechanical polishing and etching.

15. (Original) The method of claim 1, further comprising forming metal/semiconductor compound regions on said gate electrode and said drain and source regions.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Original) The method of claim 1, wherein said doping of the gate electrode is performed on the basis of process parameters selected to restrict dopant penetration of the gate insulation layer.

22. (Currently Amended) A field effect transistor, comprising:

a substrate having formed thereon a semiconductor region <u>having a top surface</u>;

a drain region <u>formed on said top surface of said semiconductor region and</u> extending along a lateral direction and a height direction;

a source region <u>formed on said top surface of said semiconductor region and</u> extending along said lateral direction and said height direction; and

a gate electrode <u>formed above said top surface of said semiconductor region and</u> extending along said lateral direction and said height direction, said gate electrode laterally located between said drain region and said source region and separated from said <u>top surface of said</u> semiconductor region by a gate insulation layer, said

drain and source regions extending along said height direction at least to an upper surface of said gate electrode.

23. (Original) The field effect transistor of claim 22, wherein said gate electrode is at least partially comprised of a doped semiconductor material, whereby a peak concentration of dopants in said gate electrode is less than a peak concentration of dopants in said drain and source regions.

24. (Original) The field effect transistor of claim 23, wherein said semiconductor region is formed on an insulating layer and has an extension in the height direction in the range of approximately 5-50 nm.

25. (New) A method of forming a field effect transistor, the method comprising:

forming a recess in a semiconductor layer, said recess having a bottom surface;

forming an implantation mask in at least said recess;

forming a drain region and a source region by performing at least one ion implantation process to implant ions into said semiconductor layer adjacent said implantation mask, wherein said implantation mask substantially prevents ions from penetrating said bottom surface of said recess;

removing said implantation mask to expose said bottom surface of said recess;

forming a gate insulation layer on said exposed bottom surface of said recess;

forming a gate electrode on said gate insulation layer; and

doping said gate electrode.

26. (New) The method of claim 25, wherein forming said gate electrode includes depositing a gate electrode material above said gate insulation layer and removing excess material of said gate electrode material to form the gate electrode.

27. (New) The method of claim 25, further comprising, prior to forming said gate insulation layer, forming sidewall spacers on sidewalls of said recess that are exposed by removing said implantation mask.

28. (New) The method of claim 27, wherein a width of said sidewall spacers is controlled on the basis of a target gate length for said gate electrode.

29. (New) The method of claim 25, wherein said implantation mask is removed by an isotropic etch process.

30. (New) The method of claim 25, further comprising forming metal/semiconductor compound regions on said gate electrode and said drain and source regions.

31. (New) The method of claim 25, wherein a lateral dimension of said recess is greater than a target gate length of said gate electrode.

32. (New) The method of claim 25, wherein said recess is formed by anisotropically etching said semiconductor layer.